REMARKS

In response to the Office Action dated May 2, 2007, Applicant respectfully requests reconsideration based on the attached amendment and the following remarks. Applicant respectfully submits that the claims as presented herein are in condition for allowance.

Claims 1-3, 7-11, 13-18, 33 and 36-38 are pending in the present application. Claims 37-38 have been withdrawn. Claims 1, 13 and 33 have been amended. New claim 39 has been added, while claim 10 has been canceled. No new matter has been added by the amendments or new claim. Applicant respectfully requests reconsideration of claims 1-3, 7-9, 11, 13-18, 33, 36 and 39 based upon the amendments and at least the following remarks.

Claim Rejections Under 35 U.S.C. § 103

In order for an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996). See MPEP 2143.

Claims 1-3, 7-11 and 36 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Tsutomu (Japanese Patent No. 2001-296523, hereinafter "Tsutomu") in view of Yoshida et al. (U.S. Patent No. 6,542,212, hereinafter "Yoshida"). Specifically, the Examiner states that Tsutomu discloses, in FIGS. 1 and 7, all of the elements of claim 1 except *each pixel including a pixel electrode and a switching element, and wherein a portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a line width larger than a width of other portions of the respective gate and data lines*, which the Examiner states is taught by Yoshida, primarily in FIG. 6 and column 8, lines 25-45. The

Examiner has further stated on page 3 of the Office action that Kim, et al. (U.S. Patent No. 6,198,516, hereinafter "Kim") teaches gate and source electrodes as being "part of" gate and data lines, respectively. Applicant respectfully traverses for at least the following reasons.

It is respectfully noted that, as the Examiner points out on page 4 of the Office action, when viewing a width of a data line strictly along an "east/west direction" with respect to FIG. 6 of Yoshida, the width varies, i.e., becomes thicker, in the east/west direction to form a drain electrode (item 42 of FIG. 6). The same concept is true regarding a variation in width in a north/south direction of gate lines to form a gate electrode (item 40 in FIG. 6). However, the variations in width of the data and gate lines as disclosed in Yoshida apply only to the width variations of data and gate lines associated only with drain and gate electrodes, respectively. In contrast and in accordance with the present invention, amended claim 1 discloses wherein a first portion of each gate line has a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data line has a first line width larger than a width of other portions of the respective data line to form a source electrode and wherein a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines, e.g., claim 1 discloses variations in width of data and gate lines associated with source and gate electrodes, respectively, as well as separate and distinct variations in width of the data and gate lines located adjacent to the white pixel.

Further, the variations in width of the data and gate lines as disclosed in Yoshida are common to all pixels of the invention in Yoshida. Specifically, FIGS. 4 and 5 of Yoshida disclose red, green and blue pixels, all having identical physical arrangement of components thereof. Yoshida does not teach or suggest any variation in physical layout of components of different pixels. Further, Applicant respectfully notes that Yoshida does not teach or suggest any fourth, e.g., white, pixels, nor does Yoshida teach or suggest variations in width of the data and gate lines, separate and distinct from variations in width of data and gate lines associated with source and gate electrodes, respectively, located adjacent to a white pixel.

Therefore, neither Tsutomu nor Yoshida, either alone or in combination, teach or suggest wherein a first portion of each gate line has a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data

line has a first line width larger than a width of other portions of the respective data line to form a source electrode and wherein a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines, as in amended independent claim 1 and similarly claimed in amended independent claims 13 and 33.

Further, neither Tsutomu nor Yoshida teach or suggest wherein a first portion of each gate line has a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data line has a first line width larger than a width of other portions of the respective data line to form a source electrode and wherein a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines.

Finally, there is no suggestion or motivation in either Tsutomu or Yoshida that a first portion of each gate line having a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data line having a first line width larger than a width of other portions of the respective data line to form a source electrode and wherein a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines would provide an advantage over the inventions taught in Tsutomu and/or Yoshida.

Thus, Applicant respectfully submits that claim 1 and claims depending therefrom, i.e., claims 2-3, 7-11 and 36, of the present invention are patentable over the cited references.

Accordingly, it is respectfully submitted that the rejection of claims 1-3, 7-9, 11 and 36 under 35 U.S.C. § 103(a) be withdrawn. Note that claim 10 has been canceled.

Claims 13 and 33 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Tanioka (U.S. Patent No. 5,929,843, hereinafter "Tanioka") in view of Yoshida. The Examiner states that Tanioka discloses all of the elements of claims 13 and 33 except *where a portion of at least one of the gate lines and the data lines located adjacent to*

the white pixel has a line width larger than a width of other portions of the respective gate and data lines, which the Examiner states is disclosed primarily in FIG. 6 of Yoshida. Applicant respectfully traverses for at least the following reasons.

As discussed above, the variations in width of the data and gate lines as disclosed in Yoshida apply to the width variations of data and gate lines associated only with drain and gate electrodes, respectively. In contrast and in accordance with the present invention, amended claim 1 discloses wherein a first portion of each gate line has a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data line has a first line width larger than a width of other portions of the respective data line to form a source electrode and wherein a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines, e.g., claim 1 discloses variations in width of data and gate lines associated with source and gate electrodes, respectively, as well as separate and distinct variations in width of the data and gate lines located adjacent to the white pixel.

Further, the variations in width of the data and gate lines as disclosed in Yoshida are common to all pixels of the invention in Yoshida. Specifically, FIGS. 4 and 5 of Yoshida disclose red, green and blue pixels, all having identical physical arrangement of components thereof. Yoshida does not teach or suggest any variation in physical layout of components of different pixels. Further, Applicant respectfully reiterates that Yoshida does not teach or suggest any fourth, e.g., white, pixels, nor does Yoshida teach or suggest variations in width of the data and gate lines, separate and distinct from variations in width of data and gate lines associated with source and gate electrodes, respectively, located adjacent to a white pixel.

Therefore, neither Tanioka nor Yoshida, either alone or in combination, teach or suggest wherein a first portion of each gate line has a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data line has a first line width larger than a width of other portions of the respective data line to form a source electrode and wherein a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the

respective gate and data lines, as in amended independent claim 1 and similarly claimed in amended independent claims 13 and 33.

Further, neither Tanioka nor Yoshida teach or suggest wherein a first portion of each gate line has a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data line has a first line width larger than a width of other portions of the respective data line to form a source electrode and wherein a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines.

Finally, there is no suggestion or motivation in either Tanioka or Yoshida that a first portion of each gate line having a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data line having a first line width larger than a width of other portions of the respective data line to form a source electrode and wherein a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines would provide an advantage over the inventions taught in Tanioka and/or Yoshida.

Thus, Applicant respectfully submits that claims 13 and 33, and claims depending therefrom, i.e., claims 14-18, of the present invention are patentable over the cited references.

Accordingly, it is respectfully submitted that the rejection of claims 13 and 33 under 35 U.S.C. § 103(a) be withdrawn.

Claims 14 and 18 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Tanioka in view of Yoshida and in further view of Morita (U.S. Patent Application No. 2002/0196243, hereinafter "Morita"). Specifically, the Examiner states that Tanioka in view of Yoshida discloses all of the elements of claim 14 except *supplying the image signals to the data driver in synchronization with a clock; and a clock generator generating the clock, the data driver operating in synchronization with the clock*, which the Examiner further states is disclosed primarily in paragraph 239 of Morita. Applicant respectfully traverses for at least the following reasons.

It is respectfully submitted that claims 14 and 18 depend from claim 13, which is submitted as being allowable for defining over Tanioka in view of Yoshida as discussed above. Furthermore, it is respectfully submitted that use of the alleged teachings of Morita do not cure the deficiencies noted above with respect to Tanioka and Yoshida.

More specifically, neither Tanioka, Yoshida nor Morita, either alone or in combination teach or suggest wherein a first portion of each a first portion of each gate line has a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data line has a first line width larger than a width of other portions of the respective data line to form a source electrode and a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel has a second line width larger than a width of other portions of the respective gate lines and the data lines and smaller than the first line width of the respective gate and data lines, as in amended claim 13, from which claim 14 depends.

Finally, there is no suggestion or motivation in either Tanioka, Yoshida or Morita that a first portion of each gate line having a first line width larger than a width of other portions of the respective gate line to form a gate electrode, a first portion of each data line having a first line width larger than a width of other portions of the respective data line to form a source electrode and wherein a second portion of at least one of the gate lines and the data lines located adjacent to the white pixel have a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines would provide an advantage over the inventions taught in Tanioka, Yoshida and/or Morita.

Therefore, it is respectfully submitted that claim 14, including claims depending therefrom, i.e., claims 15-18, define over Tanioka in view of Yoshida in further view of Morita.

Accordingly, it is respectfully requested that the rejection to claims 14 and 18 under 35 U.S.C. § 103(a) be withdrawn.

Allowable Subject Matter

Claims 15-17 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claims and

any intervening claims. Applicant gratefully acknowledges the Examiner's noting the allowable subject matter in claims 15-17, but Applicant respectfully submits that claims 15-17 are allowable as depending upon allowable independent claim 13. As such, Applicant has not rewritten claims 15-17 in independent form at this time.

Conclusion

In view of the foregoing remarks distinguishing the prior art of record, Applicant submits that this application is in condition for allowance. Early notification to this effect is requested. The Examiner is invited to contact Applicant's Attorneys at the below-listed telephone number regarding this Amendment or otherwise regarding the present application in order to address any questions or remaining issues concerning the same. If there are any charges due in connection with this response, please charge them to Deposit Account 06-1130.

Respectfully submitted,

CANTOR COLBURN LLP

By: /James J. Merrick/
James J. Merrick 43,801
Confirmation No. 5378
CANTOR COLBURN LLP
55 Griffin Road South
Bloomfield, CT 06002
Telephone (860) 286-2929
Facsimile (860) 286-0115

Date: July 31, 2007